**Detailed proposal**

1. **\* Please provide details of your proposed research to include (a) aims, objectives and central research questions of the project, (b) how existing literature on the topic has been used to inform the proposal and (c) how the project will advance state of the art and make a contribution to existing knowledge: 500 words**

(a) Aims, Objectives, and Central Research Questions:

The primary objective of this research is to optimize the Network-on-Chip (NoC) architecture in AI accelerators, particularly focusing on AMD’s VERSAL platform, to elevate the performance of Multi-Processor System-on-Chip (MPSoC), and ultimately to augment the quality of streaming media. In light of the considerable bandwidth and low latency demands of multimedia streaming, it is imperative to optimize NoC within MPSoC systems.

The objective is to develop tools and methodologies to:

1. Benchmark the NoC interconnect to identify any performance bottlenecks that may rise in media streaming within MPSoC systems.

2. Determine the optimal NoC configuration parameters to minimize latency and maximize throughput for multimedia data processing across multiple cores.

3. Perform an energy-performance trade-off analysis for streaming applications to optimize speed and power consumption in MPSoC environments.

4. Investigate potential optimizations in data transfer formats and precision across processing units while maintaining the requisite streaming quality and AI model accuracy.

The central research questions are as follows:

1. What modifications to the NoC configuration in VERSAL AI accelerators can be made to reduce latency and improve throughput in media streaming tasks within MPSoC systems?

2. What are the performance-energy trade-offs associated with different NoC configurations for MPSoC, particularly in the context of streaming applications?

3. How can data representation formats be optimized to improve energy efficiency without compromising the quality of streaming or AI model accuracy?

(b) Existing Literature and Its Influence on the Proposal:

The extant literature shows that NoC optimization is critical for improving media streaming performance in AI accelerators, particularly within MPSoC environments. Studies on VERSAL AI engines and packet switching have highlighted the challenges of managing data transfers in high-bandwidth, low-latency environments, such as those encountered in streaming. However, the existing body of research often lacks user-driven tools capable of optimizing NoC for multi-core streaming workloads in MPSoC. Furthermore, research on energy efficiency in large-scale AI models, especially those used for high-resolution media processing, further underscores the necessity of hardware-level optimizations in MPSoC systems. This proposal builds on the aforementioned findings to develop practical tools that address the complexities of NoC configuration complexities, focusing on real-time streaming applications within MPSoC platforms.

(c) Advancing the State of the Art and Contribution to Knowledge:

This project represents a significant advancement in the state of the art, offering a novel framework for optimizing NoC in AI accelerators with the specific aim of improving MPSoC performance for streaming media applications. In contrast to existing tools that concentrate on task mapping, this research will focus on fine-tuning NoC configurations for enhanced performance, energy efficiency, and scalability in streaming applications. By examining NoC configurations, energy-performance trade-offs, and data transfer optimizations, the project introduces novel methodologies for the management of intricate workloads in MPSoC systems. The collaboration with AMD’s Versal research team will provide empirical validation, ensuring that the research outcomes are both practical and impactful. Ultimately, this research delivers scalable solutions for enhancing hardware performance in MPSoC systems, addressing the high demands of streaming media in terms of bandwidth, latency, and energy efficiency.

1. **\* Please detail the research design and methodologies to be employed in carrying out your scholarship which should be described in sufficient detail to demonstrate your thorough understanding of the research topic: 500 words**

This research employs a multi-phase approach to optimize the NoC architecture in **AMD’s VERSAL AI accelerators for MPSoC systems**, with a particular emphasis on **streaming applications**. The design is centered around sustainability by benchmarking state-of-the-art implementations and maximizing the reuse of components.

**Benchmarking the State-of-the-Art (SOTA) and Analysis**:  
In this phase, existing NoC implementations on AMD’s VERSAL platform will be benchmarked using custom profiling scripts. The evaluation of key metrics, such as latency, congestion points, and bandwidth limitations will be conducted under AI streaming workloads in an MPSoC environment. By benchmarking against current SOTA designs, the performance bottlenecks and gaps will be identified, providing critical insights into how NoC configurations affect streaming applications within MPSoC systems. The results of this analysis will inform the implementation of targeted optimizations.

**Optimization of NoC Configuration Parameters**:  
By employing tools such as BookSim2 and AMD’s NoC modeling software, the **NoC configuration parameters** such as routing algorithms, buffer sizes, and link widths will be optimized. This phase aims to reduce latency and maximize throughput for MPSoC-based streaming applications. We will leverage **genetic algorithms** and other automated search methods to efficiently explore the design space. The optimization process will prioritize sustainability by reusing existing components and ensuring that any enhancements to the NoC are seamlessly integrated with minimal changes to the current system.

**Energy-Aware Task Scheduling**:  
Building on energy-efficient scheduling methods, the **Dynamic Voltage and Frequency Scaling (DVFS)** will be implemented to optimize energy consumption. Task scheduling will balance workloads across multiple MPSoC cores, ensuring resource efficiency while adhering to system memory constraints. These optimizations will reduce power consumption and latency, tailored specifically for **streaming applications** where sustained data transfer and low latency are crucial.

**Domain-Specific Energy-Performance Trade-off Analysis**:  
An in-depth **energy-performance analysis** will be performed using AMD’s VERSAL toolkit, focusing on the balance between performance and energy consumption in streaming applications. This phase will evaluate how NoC configurations and DVFS contribute to real-time energy efficiency. The goal is to optimize energy use while maintaining high throughput, ensuring relevance for MPSoC-based streaming applications.

**Low-level Data Transfer Optimization**:  
This phase will explore **custom data encoding, compression techniques, and precision management**, specifically designed to reduce data size and bandwidth usage across the NoC. These optimizations will ensure efficient bandwidth use without compromising AI model accuracy or performance in **real-time streaming** tasks.

**Validation in the Application Domain**:  
The final phase will validate the proposed NoC optimizations in **real-world MPSoC streaming applications**, using AMD’s VERSAL hardware. We will test the system against existing interfaces to demonstrate seamless integration with minimal modifications, reinforcing sustainability objectives. Key performance metrics such as frames per second, energy per inference, and bandwidth efficiency will be measured. The goal is to validate that the NoC optimizations provide significant performance gains while maximizing component reuse and energy efficiency in streaming environments.

1. **\* Please provide a schedule to include (a) milestones and deliverables for completion of the proposed research, (b) risks that might endanger reaching these deliverables and (c) the contingency plans to be put in place in order to mitigate these risks: 500 words**

Year 1: Foundation and Setup

The initial phase will concentrate on establishing a robust foundation, entailing a comprehensive examination of the extant literature on NoC architecture within MPSoC systems, AMD VERSAL platforms, and the requirements for streaming applications. This will culminate in the production of a report delineating the research gaps, particularly in the context of streaming and sustainability. By the second quarter, the research environment will be established, including the provision of AMD VERSAL development kits and the implementation of simulation tools such as BookSim2. In the third quarter, the VERSAL NoC will be benchmarked under AI streaming workloads, resulting in the production of a baseline performance report. In the final quarter, preliminary models for optimizing the NoC for MPSoC streaming applications will be developed.

Risks: Delays in hardware access.

Mitigation: Use alternative simulation tools and maintain collaboration with AMD.

Year 2: Exploration and Optimization

In the second yeae of the programme, the emphasis will be on examing NoC configurations and developing optimization algorithms. In the first half, simulation tools will be employed to investigate routing algorithms, buffer sizes, and other NoC parameters, leading to a detailed analysis. The third quarter will be dedicated to the development of optimization algorithms to enhance NoC performance and energy efficiency for MPSoC streaming applications. In the fourth quarter, an energy-performance trade-off analysis will begin, resulting in an interim report.

Risks: Algorithm failure or insufficient computational resources.

Mitigation: Iteratively refine algorithms and seek additional computational resources through cloud services or institutional support.

Year 3: Data Transfer Optimization and Validation

In Year 3, the focus will be on the optimization of low-level data transfer and the validation of these processes. The first two quarters will involve optimizing data encoding and compression techniques to reduce bandwidth usage for real-time NoC transfers in MPSoC systems. The third quarter will integrate optimized NoC configurations into a unified framework, and the fourth quarter will then validate these configurations on AMD’s VERSAL hardware, with performance metrics such as frames per second, energy consumption, and bandwidth efficiency being measured.

Risks: Hardware limitations or insufficient performance improvements.

Mitigation: Collaborate with AMD for troubleshooting and iterative tuning to address performance issues.

Year 4: Final Evaluation and Dissemination

The fourth year of the programme will ne dedicated to the final evaluation and dissemination of the findings. The first two quarters will compare the optimized NoC performance to the baseline established in Year 1, focusing on streaming performance and sustainability. The findings will be documented in a performance evaluation report. The third quarter will focus on documenting energy efficiency improvements, and the final quarter will be devoted to the preparation of the research for publication in academic journals and submission to conferences.

Risks: Delays in finalizing research or meeting publication standards.

Mitigation: Allocate buffer time to address unforeseen challenges and seek early feedback for refinement.

1. **\* Please describe any specialist knowledge or data required to undertake your proposed research, such as language competency, technical skills or use of specialist software. If this knowledge or data is not already in place, details should be provided as to how it will be acquired over the course of the scholarship:**

This research necessitates a combination of specialized knowledge, technical expertise, and sophisticated software tools to optimize the NoC architecture in AMD VERSAL AI accelerators, particularly within MPSoC systems for streaming media applications.

Technical Skills and Knowledge:

1. Network-on-Chip (NoC) Architecture:

A comprehensive grasp of NoC design, encompassing routing algorithms, buffer management, and data flow optimization within MPSoC systems, is essential. I have a robust foundation in these domains and will further augment my expertise through experimentation and a review of the literature on NoC optimization for real-time streaming tasks.

2. Deep Learning Accelerators and Hardware Design:

Expertise in deep learning accelerators, particularly the AMD VERSAL architecture, is crucial for optimizing NoC within MPSoC systems. My background in hardware design provides a solid base, which I will further develop this through direct engagement with VERSAL development kits, focusing on streaming application optimization.

3. Data Transfer and Encoding Techniques:

Understanding data encoding and compression techniques is key to optimizing NoC data movement, especially for real-time streaming tasks in MPSoC environments. While I am familiar with basic methods, I will further deepen this knowledge through targeted experimentation and literature review on bandwidth-efficient streaming solutions.

Specialist Software and Tools:

1. Simulation Tools (e.g., BookSim, AMD NoC Modeling Software):

A proficiency in the utilization of NoC simulation tools, such as BookSim and AMD’s NoC modeling software is essential for exploring and optimizing NoC configurations. I will gain expertise through tutorials and hands-on experimentation with these tools.

2. Programming Languages (Python, C++):

Strong programming skills in Python and C++ are required for algorithm development and simulation. My proficiency in these languages allows me to efficiently implement and test NoC configurations tailored for MPSoC systems and streaming applications.

3. Power Modeling and Profiling Tools:

Familiarity with AMD’s power modeling tools is crucial for conducting energy-performance trade-off analysis. I will develop proficiency by working within AMD’s development environment, focusing on energy-efficient solutions for MPSoC-based streaming applications.

Data and Access Requirements:

1. Access to AMD VERSAL Development Kits:

Access to AMD VERSAL development kits and the HPC platform HACC is crucial for validating NoC optimizations in real-world settings. These resources are secured through a collaborative effort between AMD and ETH Zurich.

2. Literature and Documentation:

Maintain ongoing access to the latest research papers and technical documentation is essential to stay current with industry advancements, guiding the direction of the NoC optimization efforts.

By building on my current skillset and acquiring additional expertise through targeted learning, experimentation, and collaboration, I am well-positioned to undertake this research. This combination of specialized knowledge and access to necessary resources ensures the successful optimization of NoC for MPSoC systems, particularly for streaming media applications and sustainable design.

1. **\* Please outline your plans for the dissemination and knowledge exchange of your research, including publications, conference attendance, poster presentations, reports and outreach activities. Details should also be provided as to how the impact of your research will be measured:**

Publications:

The primary method of disseminating research findings will be through the publication of articles in high-impact, peer-reviewed journals, including IEEE Transactions on Computers, the ACM Transactions on Design Automation of Electronic Systems, and the Journal of Parallel and Distributed Computing. These journals address pivotal domains such as computer architecture, AI hardware, energy-efficient design, and embedded systems, rendering them optimal for sharing insights related to NoC optimization for streaming media and sustainable design. The research will be published in phases, including initial findings on NoC benchmarking for streaming workloads, progress in NoC configuration optimization for real-time tasks, energy-performance trade-off analysis, and the development of a sustainable NoC framework for AI accelerators. Each paper will provide detailed methodology and results, offering valuable insights to both academic and industrial communities.

Conference Attendance and Reporting:

Presenting at international conferences represents a crucial component of the dissemination strategy. I intend to submit papers and present findings at conferences such as the IEEE/ACM International Networks-on-Chip Symposium (NoCS), the International Conference on Field-Programmable Logic and Applications (FPL), and the Design Automation Conference (DAC). These conferences are ideal platforms for sharing research findings in NoC for AI streaming applications, as well as for exchanging knowledge with experts and industry professionals. The feedback received from these conferences will assist in the refinement of the research, while fostering collaboration opportunities with peers in the field.

Poster Presentations and Workshops:

In addition to oral presentations, poster sessions at events such as the IEEE Symposium on High-Performance Computing Architecture (HPCA) will facilitate direct interaction with researchers, allowing for the exchange of ideas and the development of new connections within the scientific community. These platforms are crucial for the dissemination of research on sustainable NoC designs for real-time multimedia applications. Furthermore, participation in workshops concentrated on AI accelerators and hardware optimization will further facilitate the dissemination of findings and encourage in-depth discussions, while also exploring potential real-world applications.

Reporting and Industry Collaboration:

Regular progress reports will be disseminated to partners, particularly the AMD Versal research team, and will include detailed information regarding methodology, findings, and insights derived from the practical deployment of NoC optimizations. It is anticipated that these reports will encourage ongoing collaboration, with the potential to influence future product designs. Furthermore, internal seminars and webinars with industry partners will also be conducted, ensuring thte sustainable and practical application of research outcomes in industry settings.

Outreach Activities:

To extend the research’s impact, outreach will include writing articles for technology blogs and contributing to open-access platforms. These efforts will simplify the research findings, making them accessible to a broader audience, including those interested in NoC optimization for streaming media applications. Workshops and lectures within academic institutions will also be organized to promote sustainable NoC designs in courses and academic projects, inspiring future research directions.

Impact Assessment:

The impact of research will be gauged by the quality and quantity of publications, citation counts, and the feedback received from conferences and industry collaborators, particularly AMD. The adoption of NoC optimization techniques for streaming media and sustainability in both academic and industrial settings will provide further insight into the success of the research. Moreover, the impact of outreach activities will be assessed using metrics such as blog post views, open-access downloads, and audience engagement, ensuring a broader societal impact.

1. **\* Please outline your reasons for choosing your proposed (a) academic supervisor(s) and (b) higher education institution making particular reference to how the chosen supervisor and institution**

I have selected Professor Shreejith Shanker as my academic supervisor due to his expertise in computer architecture, AI hardware acceleration, and NoC design. His involvement in projects focused on energy-efficient compute flows in the media industry is closely aligned with my own research on optimizing NoC for streaming applications. Additionally, Professor Shanker’s involvement in a Horizon Europe (HEU) project investigating energy consumption in the movie industry’s compute flows complements my focus on energy-performance trade-offs in real-time streaming tasks. His extensive experience with the AMD VERSAL architecture provides invaluable insights into optimizing NoC for real-time, energy-intensive applications. Furthermore, his established collaborations with industry partners such as AMD ensure that my research will have practical relevance and access to cutting-edge resources. Under his supervision, I will receive guidance that integrates both academic rigor and industrial applications, which is essential for the success of my research.

Trinity College Dublin (TCD) offers an ideal platform for my research, distinguished by its reputation for excellence in engineering, AI, and computer architecture. The School of Computer Science and Statistics provides access to cutting-edge facilities, including AMD VERSAL platforms, which are essential for my NoC optimization efforts. TCD’s involvement in Horizon Europe projects related to sustainable computing in media applications aligns perfectly with my focus on energy-efficient NoC designs for streaming tasks. Moreover, TCD’s strong partnerships with industry leaders such as AMD will facilitate valuable collaboration, allowing my research to tackle both theoretical and practical challenges. TCD’s dynamic research community encourages innovation and societal impact, ensuring that my work contributes to the expanding field of AI hardware optimization.

By selecting Professor Shreejith Shanker and Trinity College Dublin, I will benefit from exceptional mentorship, cutting-edge resources, and industry connections, all of which are crucial for advancing my research on NoC optimization for AI accelerators, particularly in the areas of streaming media and sustainable design. This combination of expertise and support will ensure that my research makes a significant contribution to both academic knowledge and industrial practice.

1. **\* Please provide details of any proposed research trip(s) of more than four weeks duration which you believe will be necessary for the successful completion of your award:**

Proposed Local Research Trip

Location: AMD Research Lab, Dublin

Duration: 6 weeks

Objective: This research trip aims to collaborate directly with AMD's research team and gain hands-on access to the VERSAL hardware platform. Access to this hardware is critical for testing and validating the NoC optimization techniques developed in my research.

Reason for the Trip: While based at Trinity College Dublin, having extended access to AMD’s facilities will allow for hands-on experimentation with the VERSAL devices and enable real-time collaboration with AMD engineers. Such direct engagement is essential for troubleshooting and fine-tuning NoC configurations, ensuring that the research meets the requisite industry standards and real-world requirements. The six-week period will allow for uninterrupted access, facilitating comprehensive testing and validation of the proposed optimizations.

Expected Outcomes: During this six-week trip, I will conduct detailed experiments to quantify essential performance metrics such as latency, throughput, and energy efficiency on AMD’s VERSAL hardware platform. These results will be instrumental in the refinement of NoC optimization techniques and providing real-world validation for my research, ensuring that the methods are both academically rigorous and industrially relevant.

Contribution to the Project: This research trip is a vital component of my project. It enables me to test the NoC optimizations directly on industry-grade hardware and receive immediate feedback from AMD engineers. This collaboration will guarantee that the optimization techniques developed are not only theoretical but also practical and impactful for AI hardware optimization.

This local research trip will provide indispensable resources and expertise, ensuring the successful completion of my project.